UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,886	12/26/2001	Jung-Won Suh	29926/38065	4259

4743 7590 04/04/2005

MARSHALL, GERSTEIN & BORUN LLP
6300 SEARS TOWER
233 S. WACKER DRIVE
CHICAGO, IL 60606

EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,886	SUH, JUNG-WON	
	Examiner	Art Unit	
	Midys Inoa	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/17/04 has been entered.

Response to Arguments

2. Applicant's arguments, see pages 4-7, filed on 8/17/04, with respect to the rejection(s)of claim(s) 1-2, and 4-7 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Sakurai (5,999,472) in view of Verbanets, Jr. et al. (4,974,199).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 and 4-9 are rejected under 35 U.S.C. 103(a) as being obvious over Sakurai (5,999,472) in view of Verbanets, Jr. et al. (4,974,199).

Regarding Claim 1, Sakurai discloses an apparatus for controlling a bank ("memory bank 1") refresh including a plurality of banks ("array banks 0-3", Col. 8, lines 7-18), comprising: an input buffer means for buffering bank address signals inputted from an external circuit with the command signal (input buffer 7 and address buffer 106);

a reset control unit ("refresh control circuit 18") for receiving output signals from the plurality of input buffer means to thereby generate a reset (or refresh) signal (Col. 8, lines 33-50)

a counter for producing count signals (refresh counter 9);

a switch means for combining (MUX 10) the count signals from the counter (refresh counter 9) in order to produce internal bank refresh signals in response to bank address signals from the [N] plurality of input buffer means; and

a chipset control means (refresh control 18) for generating a plurality of internal bank addresses (RADi) for the refresh using the internal bank refresh signals (fmx).

Sakurai does not teach the counter being reset by the reset signals and the reset control unit including a NOR gate for combining the output signals from the plurality of input buffer means. Verbantes discloses a NOR gate and an inverter that together allow for the resetting of a counter (Col. 39, line 43 – Col. 40, line 9). It would have been obvious to one of ordinary skill in the art to allow the counter of Sakurai to be reset as that of Verbantes thus giving the system the ability to return the counter to an original state in case of an operating error.

Regarding Claim 2, Sakurai does not specify the number of banks ("memory arrays") or buffering means, however, the system can be configured to comprise a plurality of banks as well as a plurality of buffer means. Therefore, the number of input buffer means can be N, the refresh counter 9 can be (N-1)-nary to accommodate N input buffer means, and the number of banks can be 2N, according to the number of buffer means needed (Column 19, line 46-Column 20, line 47).

Regarding Claim 4, Sakurai discloses the (N-1)-nary counter (refresh counter 9) is reset by a logic combination of the bank address signals (fr), which is produced from the combination

of output signals from the control signal buffer 7 after being decoded by the command decoder 5 (See Figure 15).

Regarding Claims 5-7, Sakurai discloses a method for controlling a bank refresh including 2^N of banks ("memory bank 1", "array banks 0-3", Col. 8, lines 7-18), comprising the steps of:

buffering N bank address signals inputted from the external circuit with the refresh command signals (Column 20, lines 11-27) ;

outputting the (N-1)-nary count signal in sequence by inputting a reset signal (Column 19, lines 38-45);

switching and outputting unit of N-1 count signals to the bank refresh combination signals in response to the N buffered signals; and

generating an internal bank address for the refresh using the bank refresh combination signals (Column 19, lines 15-37).

Although Sakurai discloses 4 banks (array banks 0-3) banks, the system can be configured to comprise any plurality of banks as well as a plurality of buffer means (See Figure 15 and Column 19, line 46-Column 20, line 47). Therefore, the number of input buffer means can be N, the refresh counter 9 can be (N-1)-nary to accommodate N input buffer means, and the number of banks can be 2N, according to the number of buffer means needed. N can take any value, including 3, which is a positive integer. With N being 3, the system would still operate properly.

In buffering the bank signals with the refresh command signals, the bank address signal ADi and the refresh command signals (fmx and RADi) are taken in by a row address latch circuit, which in turn acts as a buffer.

Sakurai does not disclose generating a reset signal based in the logic NOR operation of the N buffered bank address signals. Verbantes discloses a NOR gate and an inverter that together allow for the resetting of a counter (Col. 39, line 43 – Col. 40, line 9). It would have been obvious to one of ordinary skill in the art to allow the counter of Sakurai to be reset as that of Verbantes thus giving the system the ability to return the counter to an original state in case of an operating error.

Regarding Claim 8, Sakurai discloses a latch means (latch circuit 103) sustains the output signals of the plurality of input buffer means within a certain period of time only when the refresh command signals are applied (Column 9, line 10-37). In Sakurai's system, the latch means is not inside of the buffer means, however, it is part of the buffer/reset system. Additionally, other latch means can also be present within the buffer means (in addition to 103) since buffers are known to include latches in their structure.

Regarding Claim 9, Verbantes discloses the apparatus wherein the reset control unit further includes an inverter for inverting an output signal from the NOR gate (Col. 39, line 43 – Col. 40, line 9).

Conclusion

4. The prior art made of record and relied upon is considered pertinent to applicant's disclosure.

- Verbanets, Jr. et al. (4,974,199) Digital IC-Microcomputer Interface

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 1, 2005

Midys Inoa
Midys Inoa
Examiner
Art Unit 2189

MI

Pierre Vital
Pierre Vital
Primary Examiner
Art Unit 2188